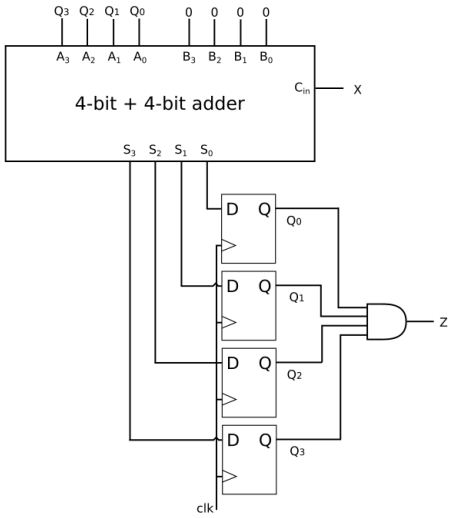
Consider the circuit below with input X and output Z. Note that the nodes labeled 'Q' are internal to the system (they are not inputs or outputs). Timing parameters for the components are listed in the table.



Tp NAND	10ns
Tp ADDER	100ns
Tp DFF	20ns
Tsu DFF	5ns
Th DFF	2ns

a)

Assume that a rising clock edge occurs at time t=0. At what times does input X need to be stable?

Causing a change on X will cause a change at the flip-flop inputs after the adder's propagation delay. Around the clock edge in question, the setup and hold time for the flip-flops span from t = -5 ns to +2 ns, so the D inputs should not change during that time. That means that X should be stable from t = -105 ns to -98 ns.

b)

Assume that a rising clock edge occurs at time t=0. At what time do you expect the output to be correct?

That clock edge will cause changes through the flip-flops (which all happen together), which will cause changes through the AND gate, which will change Z. So, the output is expected to update at t=30 ns.

c)

What is the maximum frequency at which the flip-flops can be clocked and the circuit still behave as intended? Leave your answer as a mathematical expression in terms of the given timing parameters.

After a clock edge, it will take $T_{PDFF}+T_{PADDER}$ before the D inputs of the flip-flops are done changing. They need to remain stable for the setup time before another clock edge can occur. So $fmax = \frac{1}{T_{PDFF}+T_{PADDER}+T_{SU}}$

d)

Assume that the adder is a ripple-carry adder (where the carry for each lower place value feeds into the next place value). As you increase the frequency of the clock *just* to the point where the circuit stops behaving as intended, which flip-flop's value would you expect to be incorrect?

The longest propagation delay would be to the adder's output S_3, so Q_3 would be expected to be incorrect.