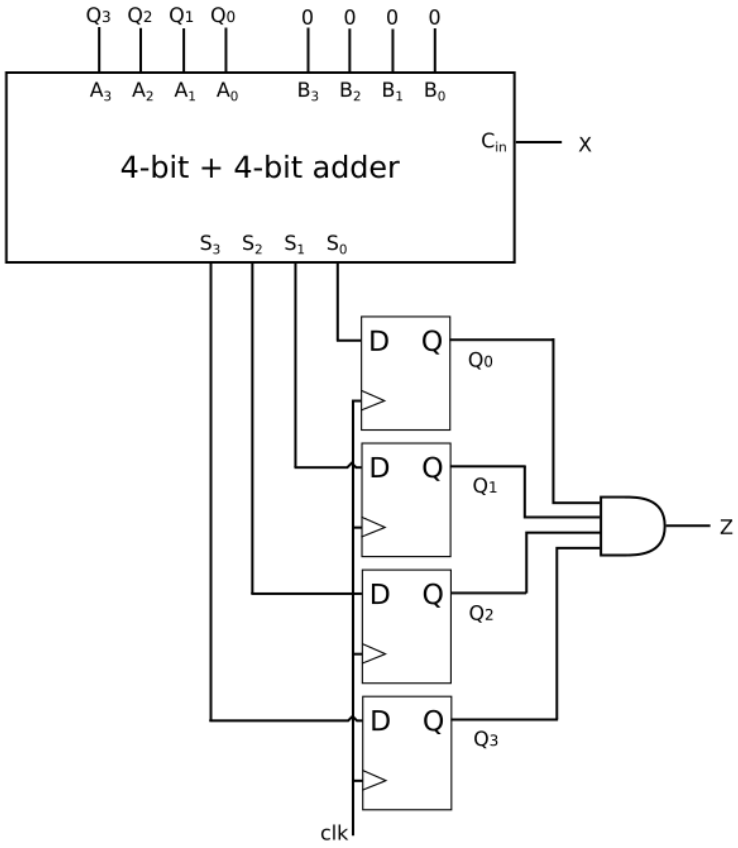
Consider the circuit below with input X and output Z. Note that the nodes labeled 'Q' are internal to the system (they are not inputs or outputs). Timing parameters for the components are listed in the table.



Tp NAND	10ns
Tp ADDER	100ns
Tp DFF	20ns
Tsu DFF	5ns
Th DFF	2ns

a)
Assume that a rising clock edge occurs at time t=0. At what times does input X need to be stable?

b)
Assume that a rising clock edge occurs at time t=0. At what time do you expect the output to be correct?

c)
What is the maximum frequency at which the flip-flops can be clocked and the circuit still behave as intended? Leave your answer as a mathematical expression in terms of the given timing parameters.

d)
Assume that the adder is a ripple-carry adder (where the carry for each lower place value feeds into the next place value). As you increase the frequency of the clock *just* to the point where the circuit stops behaving as intended, which flip-flop's value would you expect to be incorrect?