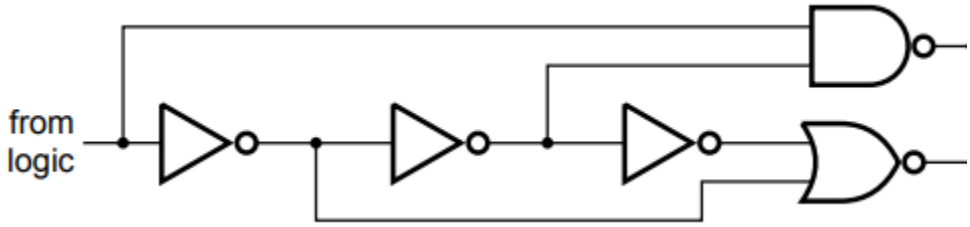
Observe Figure 3 in this datasheet:
https://assets.nexperia.com/documents/data-sheet/74HC_HCT4052.pdf

The relevant logic for this problem is reproduced here:



For convenience, call the input to the circuit (labeled “from logic” above) “FL”, the output of the NAND gate “A” and the output of the NOR gate “B”.

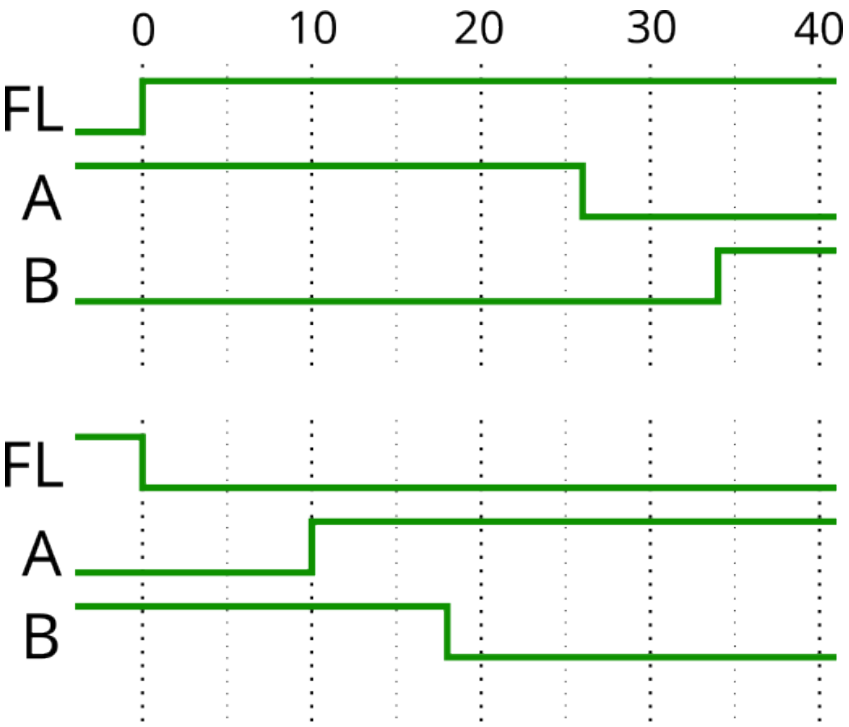
a) Write simplified Boolean expressions (i.e. simplify the expressions as much as possible) for A and B in terms of FL.

$$A = \overline{FL}$$

$$B = FL$$

b) Create two timing waveforms, each with FL, A, and B. Draw them one above the other and at the same scale so that you can compare the behavior in each case. In the top one, simulate FL transitioning from low to high at t=0, and in the bottom one, transitioning from high to low at t=0. Simulate over a relevant time span based on these timing specifications:

Gate	Propagation delay
NOT	8 ns
NAND	10 ns
NOR	10 ns



c) In the "Features and benefits" section of the datasheet is the phrase "'break before make' built-in". Don't worry about the specifics, but assume that there are several of the logic circuits above, and the outputs of each circuit (both A and B working together) control electronic switches (one switch controlled by each of these circuits). In this context, "make" means to close a switch and "break" means to open a switch.

Are the switches that these circuits control open when the 'from logic' signal is high or low?

Since all of the changes caused by FL going low happen faster than all of the changes caused by FL going high, FL going low must be what "breaks" the connection (opens the switch), so the switches are open when FL is low.