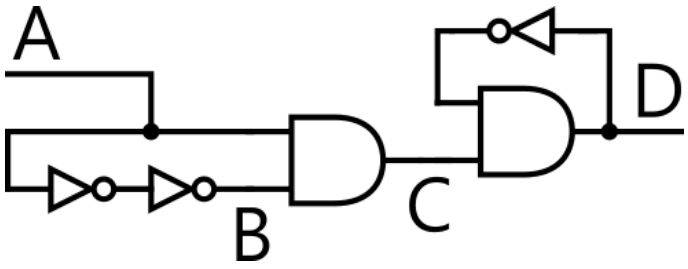

Complete the timing simulation below for nodes B, C, and D in the circuit above using the timing parameters T_{PNOT}=3 ns and T_{PAND}=5 ns. Include annotations for the time of each transition, as is done on signal A. There is room at the bottom for additional nodes if desired.

Notes:

- **B can be determined all at once based on A, which is already known. It is logically equivalent to A, so it does the same thing as A, but is delayed by two inverters (6 ns).**
- **C can then be determined all at once based on A and B (pun intended).**
- **D cannot be determined all at once because it depends on itself. The node /D needs to be simulated alongside D, filling in each as the simulation progresses.**
    - **For example, at the beginning of the simulation, C is low, so D is low, so /D is high. Once C goes high, D will go high 5 ns later, causing /D to go low 3 ns after that.**