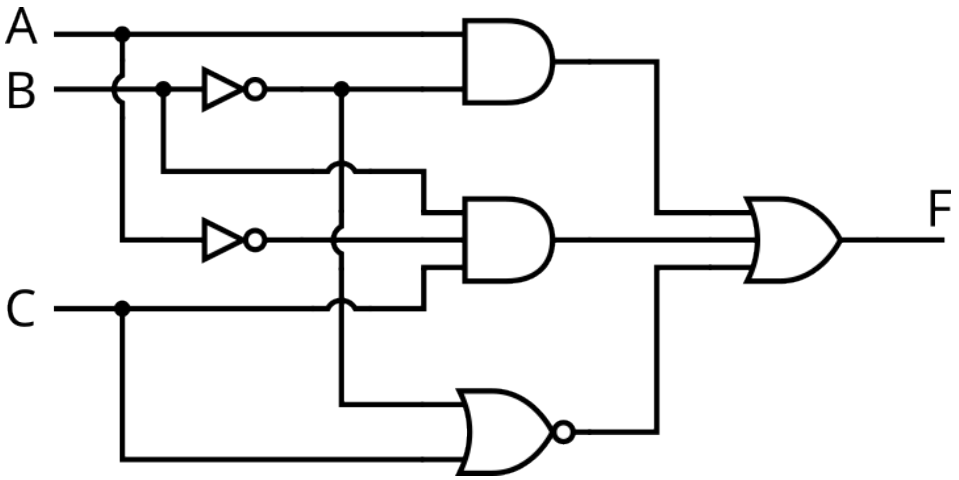
a) Write the Boolean expression that the following gate schematic implements.



b) Starting with the expression above, draw a starting point for mixed-logic schematic manipulation, then perform a manipulation to create an implementation that uses only NAND gates and inverters.

c) How many inverters does the result of b) require?