Design a CMOS gate (as a transistor-level schematic) that produces output Y according to

$$Y = (\overline{A} + \overline{B + \overline{C}}) \cdot \overline{D}$$

Label FET gates with complemented input signals if needed.

$$pullup = (\overline{A} + \overline{B} \cdot C) \cdot \overline{D}$$

$$pulldown = A \cdot \left(B + \overline{C}\right) + D$$