Registers and Latches

Part A Implement a transparent latch using only four 2-input NAND gates and one inverter. Label \textit{in}, \textit{out}, and \textit{enable} signals. Use correct mixed logic notation.

\[
\begin{array}{c}
\text{In} \quad \rightarrow \quad \text{NAND} \quad \rightarrow \quad \text{NAND} \quad \rightarrow \quad \text{NAND} \quad \rightarrow \quad \text{Inverter} \quad \rightarrow \quad \text{Out}
\end{array}
\]

Part B Implement a \textbf{register with write enable}, using only transparent latches, NAND, NOR, AND, OR, and NOT gates. Use mixed logic design methodology. You do \textbf{not} have to implement transparent latches from basic gates. Label input and output signals \textit{INPUT}, \textit{WE}, \textit{Phi}1, \textit{Phi}2, and \textit{OUTPUT}. Label the output of the first latch as \textit{X}.

\[
\begin{array}{c}
\text{In} \quad \rightarrow \quad \text{NAND} \quad \rightarrow \quad \text{NAND} \quad \rightarrow \quad \text{NAND} \quad \rightarrow \quad \text{Inverter} \quad \rightarrow \quad \text{Out}
\end{array}
\]

Part C Now \textbf{complete the timing diagram} for this register based on the specified inputs. Point \textit{X} is defined as the output of the first latch in the register. \textit{OUT} is the output of the register. Assume all internal storage is initially zero. Ignore gate propagation delay.