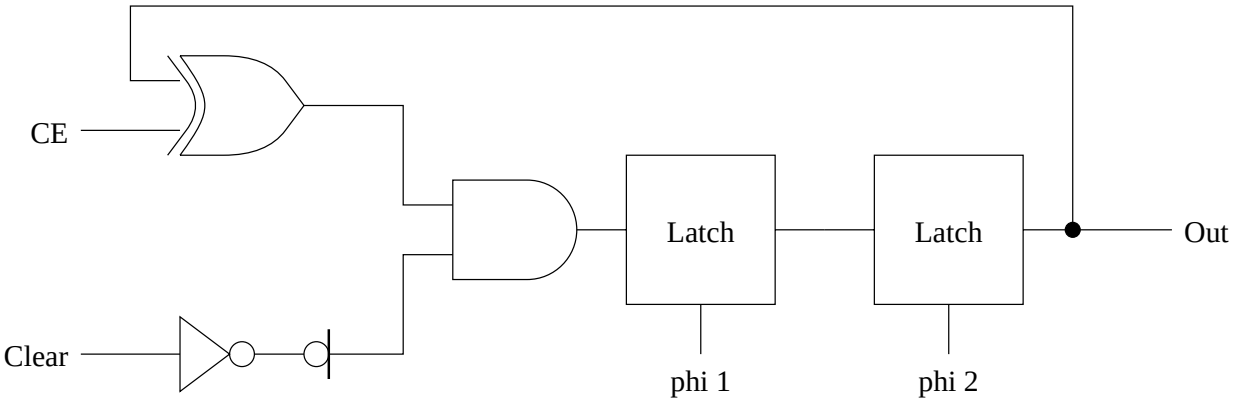
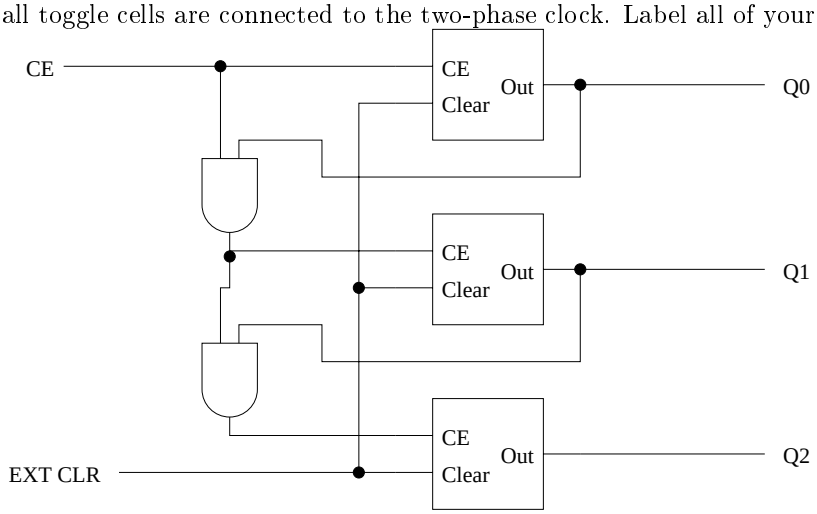
Counter Design

Part A Design a toggle cell using transparent latches, 2-input XOR gates, and 2-input basic gates (AND, OR, NAND, NOR, and NOT). Include a toggle enable CE, active high clear CLR, and a two-phase non-overlapping clock. You should have a single output OUT.



Part B Now use several of your toggle cells (in icon form) to build a divide by eight counter. This design should include a count enable CE and an active high clear CLR. You do not need to draw in the clock signals. Assume all toggle cells are connected to the two-phase clock. Label all of your outputs signals.



Part C Now use your toggle cells (in icon form) to build a divide by seven counter. This design should include a count enable CE and an active high clear CLR. Your design should clear if (A) the external clear CLR is high, or (B) the maximum output count is reached and the count enable is high. You do not need to draw in the clock signals.