Cascading Counters

When cascading divide by N counters, it is necessary to modify the control of the \overline{Clear} to prevent unwanted clears (e.g., 48,49,50,01,02 in a divide by 60 counter.) Suppose a divide by N counter is built using a binary counter (cascaded toggle cells) described as follows:

Count				
Enable	\overline{Clear}	cycle	Out	
X	0	$\uparrow\downarrow$	0	clear
0	1	$\uparrow\downarrow$	Q_o	hold
1	1	$\uparrow\downarrow$	$\overline{Q_o}$	count

This problem addresses the design of logic that accepts as inputs:

 $\begin{array}{ll} Count \, Enable & \text{ allows divide by N counter to count} \\ External \, Clear & \text{ clears divide by N counter (active high)} \end{array}$

Max. Count indicating the maximum count (N-1) is currently output

The single output, \overline{Clear} , drives the binary counter clear signal.

Part A Complete the truth table below to describe the logic which prevents the unwanted clears mentioned above.

$External \ Clear$	Count	Max.	
Clear	Enable	Count	\overline{Clear}
0	0	X	
0	1	0	
0	1	1	
1	X	X	

Part B Now determine a simplified expression for \overline{Clear} by completing the Karnaugh Map, circling the prime implicants, and writing a simplified expression.

	Count Enab	le Count Enable	prime implicant	essential?
Ext. Clear {				yes□ no□
Ext. Clear				yes□ no□
-				yes no
N	Iax. Count N	Iax. Count Max. Cour	nt	
	\overline{Clean}	·		

Part C Implement this simplified expression using a mixed logic design methodology. Be sure and label the inputs $External\ Clear$, $Count\ Enable$, and $Max.\ Count$, and the output, \overline{Clear} .