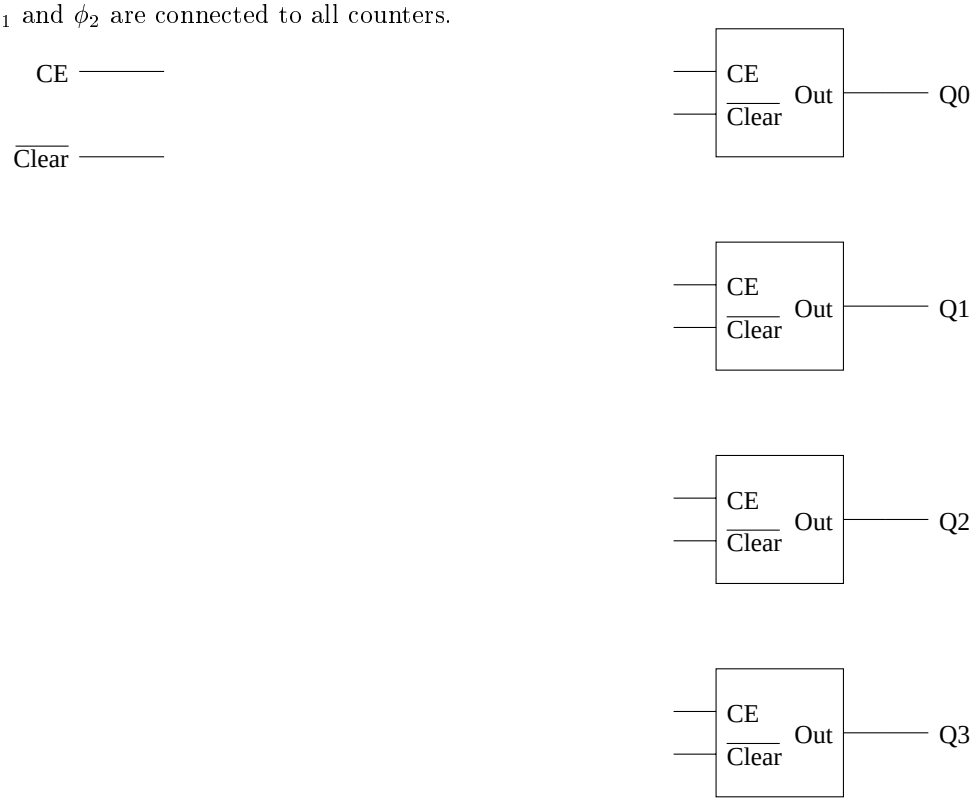
Counters

Part A Design a one bit counter, described in the truth table below, using AND, OR, NAND, NOR, NOT, XOR, and XNOR, gates, *plus* transparent latches. Use an icon for the latches. You do not need to show the implementation of the latches. Be sure to label the signals: CE, $\overline{Clear}$, Out, ϕ_1, and ϕ_2.

$CountEnable$	Out_{old}	$\overline{Clear}$	$cycle$	Out_{new}
X	X	0	$\uparrow\downarrow$	0
0	0	1	$\uparrow\downarrow$	0
0	1	1	$\uparrow\downarrow$	1
1	0	1	$\uparrow\downarrow$	1
1	1	1	$\uparrow\downarrow$	0

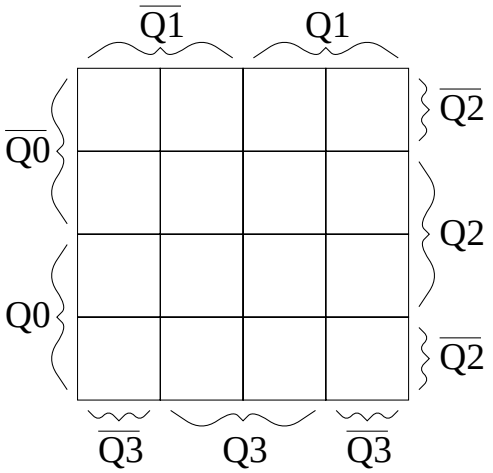
Part B Design a four-bit binary counter (divide by 16) using the counters below plus AND, OR, NAND, NOR, NOT, XOR and XNOR gates. The CE (count enable) and $\overline{Clear}$ should work for *all* counters. Assume ϕ_1 and ϕ_2 are connected to all counters.



Part C To create a divide by ten counter, logic must be created to detect the 1001 output case and bring low the $\overline{Clear}$ signal. Use a Karnaugh map to determine the simplified expression for the following truth table. Circle all prime implicants.

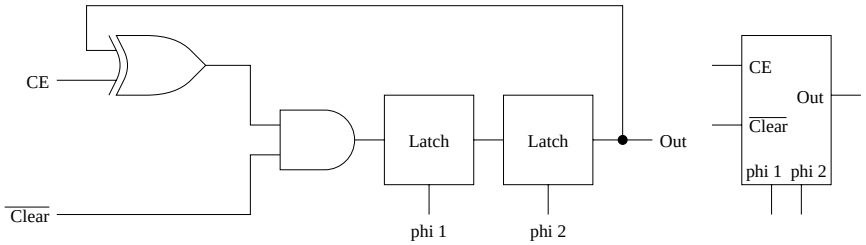
Q3	Q2	Q1	Q0	$\overline{\text{Clear}}$
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1

Q3	Q2	Q1	Q0	$\overline{\text{Clear}}$
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



$\overline{Clear} =$ _____

Part D A one bit counter (toggle cell) is implemented below. Use the icon shown below to implement a divide by eight counter using this cell (drawn in icon form) plus AND, OR, NAND, NOR, NOT, XOR and XNOR gates. The CE (count enable) and $\overline{Clear}$ should work for *all* counters.



Part E Now modify the toggle cell design so that the $Clear$ is active high (i.e., it clears when the input is a '1'), and it only clears when the count enable signal (CE) is high. The truth table below summarizes this behavior. Use mixed logic design methodology. Draw the implementation of a divide by two counter.

$CountEnable$	$Clear$	Out_{old}	$cycle$	Out_{new}
0	X	Q_o	$\uparrow\downarrow$	Q_o
1	0	Q_o	$\uparrow\downarrow$	$\overline{Q_o}$
1	1	Q_o	$\uparrow\downarrow$	0