Mixed Logic Understanding

Part A You have obtained the following schematics with no description of their operation. Fortunately, the designer used a mixed logic design strategy.

\[ F_{(A,B,C,D,E,F)} = \]

Part B Express the function computed by this circuit.

\[ F_{(A,B,C,D)} = \]

Part C Express the function computed by this circuit.

\[ F_{(A,B,C,D,E)} = \]

Part D How many transistors are required for the circuit implementation above?

number of transistors =

Part E Now change the implementation to use NAND and NOT gates. Accomplish this only by adding buffers and changing bubble pairs.
Part F How many transistors are required for the new implementation?

number of transistors = ____________________________

Part G Express the function computed by this circuit.

\[ F_{A,B,C,D} = \] ____________________________

Part H How many transistors are required for the circuit implementation above?

number of transistors = ____________________________

Part I Now change the implementation to use NOR and NOT gates. Accomplish this only by adding buffers and changing bubble pairs.

Part J How many transistors are required for the new implementation?

number of transistors = ____________________________
**Part K** Express the function computed by this circuit.

\[
F_{(A,B,C,D,E,F,G)} = \quad \text{[Function Expression]}
\]

**Part L** How many transistors are required for the circuit implementation above?

number of transistors = \quad \text{[Number]}  

**Part M** Now change the implementation to use 2-input and 3-input NOR and NOT gates. Accomplish this only by adding buffers and changing bubble pairs.