Gate-Level Circuit Design

For each expression below, create a gate level implementation using only the specified types of gate. Use mixed logic notation (i.e., bubbled output go to bubbled inputs and non-bubbled outputs go to non-bubbled inputs). Do not assume you have the complements of the inputs.

\[ \text{Out} = AB + BC \text{ using only NAND gates} \quad \text{Out} = (A + B)(C + D) \text{ using only NOR gates} \]

\[ \text{Out} = A + BC \text{ using only NAND and NOT gates} \quad \text{Out} = (A + B)(C + D) \text{ using only NOR gates} \]

\[ \text{Out} = A \oplus B \text{ using NAND and NOT gates} \quad \text{Out} = AB + C(D + E) \text{ using NAND and NOT gates} \]

\[ \text{Out} = A \oplus B \text{ using NOR and NOT gates} \quad \text{Out} = (A + B)(C \overline{D} + E) \text{ using NOR and NOT gates} \]