Problem 1 (20 points) For the bit representations below, determine the most negative value, most positive value, and step size (difference between sequential values). All answers must be expressed in decimal notation just like the practice problems we did in class (using k, M notation). Fractions (for example 3/16ths) must be used. All signed representations are two's complement signed numbers. You must show your work.

<table>
<thead>
<tr>
<th>representation</th>
<th>most negative value</th>
<th>most positive value</th>
<th>step size</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned integer (15 bits). (0 bits)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signed integer (15 bits). (0 bits)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>unsigned fixed-point (15 bits). (8 bits)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>signed fixed-point (15 bits). (8 bits)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Problem 2 Part A Arithmetic (10 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a five bit **unsigned** representation.

\[
\begin{array}{cc}
0 & 1 & 0 & 1 & 1 \\
+ & 1 & 1 & 0 & 0 & 1 \\
\hline
\end{array}
\quad
\begin{array}{cc}
0 & 1 & 1 & 0 & 1 \\
+ & 0 & 0 & 1 & 0 & 0 \\
\hline
\end{array}
\]

result

unsigned
error?

Problem 2 Part B Arithmetic (10 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a five bit **signed** two's complement representation.

\[
\begin{array}{cc}
0 & 1 & 0 & 1 & 1 \\
+ & 0 & 1 & 1 & 0 & 1 \\
\end{array}
\quad
\begin{array}{cc}
1 & 0 & 1 & 1 & 1 \\
+ & 0 & 1 & 0 & 0 & 1 \\
\hline
0 & 1 & 0 & 0 & 0 \\
\end{array}
\quad
\begin{array}{cc}
1 & 0 & 0 & 1 & 1 \\
- & 0 & 0 & 1 & 0 & 1 \\
\hline
- & 0 & 0 & 1 & 1 & 0 \\
\end{array}
\]

result

signed
error?

Problem 2 part C Arithmetic (10 points) The adder below adds two four bit numbers X and Y and produces a four bit result S. Add the digital logic to support subtraction as well as addition. Label inputs X3, X2, X1, X0, Y3, Y2, Y1, Y0, as well as outputs Z3, Z2, Z1, Z0. Do not put in the circuitry to determine errors.

[Diagram of an adder]
3) (10 points) Complete the truth table for the following logic block.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

What boolean function (if any) does the circuit implement? ___________________________
4) Counters (10 points) Connect the toggle cells below to build a divide by 11 counter. Be sure to include an external Count Enable and an external active high clear. Include any circuitry needed to allow this to work in multiple digit counters (like in an alarm clock). You do not have to used mixed logic.
5) (15 points) Consider the following circuit. For each combination of inputs listed below, determine the corresponding outputs. You must show your work and reasoning for any credit. Do not just put an answer without explaining.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
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<td></td>
</tr>
</tbody>
</table>

In0 > In1 > In0 > In3

Decoder

Priority Encoder

In0 | Out0
In1 | Out1
In2 | Out2
In3 | Out3

D E F
6) Registers (15 points) Consider the register implementation below.

Assume the following signals are applied to the register above. Draw the signal at point A (output of the first latch), the signal at point OUT (output of second latch). Assume A and OUT start at unknown values which are shown below as both a high and a low at the same time with cross hatches drawn between the two values.