Problem 1 (3 parts, 25 points)

## Encoders and Decoders

Part A (6 points) Consider a priority encoder with the following behavior:

| $\mathrm{In}_{2}$ | $\mathrm{In}_{1}$ | $\mathrm{In}_{0}$ | Valid | Out $_{1}$ | Out $_{0}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | x | x |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 |

List the inputs $\left(\mathrm{In}_{0}, \mathrm{In}_{1}\right.$, and $\left.\mathrm{In}_{2}\right)$ in decreasing priority.

$$
\frac{\mathrm{In}_{1}}{\text { highest priority }}>\frac{\mathrm{In}_{0}}{\text { 2nd highest priority }}>\frac{\mathrm{In}_{2}}{\text { lowest priority }}
$$

Part B (12 points) Implement the priority encoder from part A using 2-input or 3-input NORs and inverters only.

$$
\begin{aligned}
& \text { Valid }=\mathrm{In}_{0}+\mathrm{In}_{1}+\mathrm{In}_{2} \\
& \text { Out }_{1}=\overline{\mathrm{In}}_{0} \mathrm{In}_{1} \\
& \text { Out }_{0}=\mathrm{In}_{1}
\end{aligned}
$$



Part C (7 points) Complete the circuit below to implement Out, whose behavior is shown in the truth table. Use only the decoder and one basic gate (e.g., AND, NAND, OR, NOR).


Problem 2 (3 parts, 30 points)
Part A (12 points) Convert the following notations:

| binary notation | decimal notation |
| :---: | :---: |
| 1101.011 | 13.375 |
| 1011111.1 | 95.5 |
| 011111101000 | 2024 |
| hexadecimal notation | octal notation |
| $0 \times 440$ | 2100 |
| 17.68 | 27.32 |
| $0 \times 178$ | 570 |

Part B (12 points) For the 24 bit representations below, determine the most positive value and the step size (difference between sequential values). Express all answers in decimal notation do not leave your answer as 2 raised to an exponent (e.g., say 4 K , not $2^{12}$ ). Fractions (e.g., 3/16ths) may be used. Signed representations are two's complement.

| representation | most positive value | step size |
| :---: | :---: | :---: |
| unsigned integer <br> (24 bits) . (0 bits) | $\mathbf{1 6 M}$ | $\mathbf{1}$ |
| signed fixed-point <br> (18 bits) . (6 bits) | $\mathbf{1 2 8 K}$ | $\mathbf{1 / 6 4}$ |
| signed integer <br> (24 bits) . (0 bits) | $\mathbf{8 M}$ | $\mathbf{1}$ |
| signed fixed-point <br> (20 bits) . (4 bits) | $\mathbf{5 1 2 K}$ | $\mathbf{1 / 1 6}$ |

Part C (6 points) What is the minimum number of bits needed to represent the following numbers in signed two's complement and as unsigned numbers?

| Number: | Min \# bits for signed representation: | Min \# bits for unsigned representation: |
| :---: | :---: | :---: |
| -64 | $\mathbf{7}$ | N/A |
| 1204 | $\mathbf{1 2}$ | $\mathbf{1 1}$ |
| 64 | $\mathbf{8}$ | $\mathbf{7}$ |

Problem 3 (3 parts, 30 points)
Part A (16 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a five bit unsigned and five bit two's complement representations.

|  | 10011 | 111 | 1100 | 10001 |
| :---: | :---: | :---: | :---: | :---: |
|  | +11001 | $\begin{array}{r}\text { a } \\ +\quad 1010 \\ \hline\end{array}$ | - 111 | - 10011 |
| result | 01100 | 10001 | 00101 | 11110 |
| unsigned error? | Yes | No | No | Yes |
| signed error? | Yes | Yes | No | No |

Part B (8 points) For each bit string below, what is the decimal number it represents if it uses a 5 -bit unsigned representation and if it uses a 5-bit two's complement representation?

| Bit string | Decimal (if unsigned representation) | Decimal (if 2's complement signed representation) |
| :--- | :---: | :---: |
| 10110 | $\mathbf{2 2}$ | $\mathbf{- 1 0}$ |
| 101.11 | 5.75 | $\mathbf{- 2 . 2 5}$ |

Part C (6 points) A 26 bit floating point representation has a 16 bit mantissa field, a 10 bit exponent field, and one sign bit.

What is the largest value that can be represented (closest to infinity)?

What is the smallest value that can be represented (closest to zero)?


How many decimal significant figures are supported?

Problem 4 (2 parts, 15 points)
Consider the following circuit.


Building Blocks and Pass Gates

| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{X}$ | $\mathbf{Y}$ |
| :---: | :---: | :---: | :---: |
| 0 | 0 | $\mathbf{0}$ | $\mathbf{0}$ |
| 0 | 1 | $\mathbf{0}$ | $\mathbf{0}$ |
| 1 | 0 | $\mathbf{1}$ | $\mathbf{0}$ |
| 1 | 1 | $\mathbf{0}$ | $\mathbf{1}$ |

Part A (8 points) Fill in the truth table to the right with its behavior.
Part B (7 points) What building block does this circuit implement? Express your answer in the form of n-to-m <type of building block> (e.g, 16-to-1 mux).

1-to-2 decoder

