Problem 1 ( 3 parts, 21 points)
"A chip off the old block"
Part A (15 points) Consider the five definitions for the block drawn below. One block input is the logical value $A$. The other input is the control value $C$. The output behavior for each of the five definitions is given in the table. Complete the full truth table and state the logical (gate) names for each definition. (hint: the first block one appears to mask $\boldsymbol{A}$ when its control input is low.)


| In | $C$ | $(1)$ | $(2)$ | $(3)$ | $(4)$ | $(5)$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 1 | 0 | $\mathrm{Z}_{0}$ |
| 1 | 0 | 0 | 1 | 0 | 1 | $\mathrm{Z}_{0}$ |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 |


| (1) | AND | (2) | XOR | (3) | NOR |
| :--- | :--- | :--- | :--- | :--- | :--- |
| (4) | OR | (5) | Pass Gate |  |  |

Part B (6 points) The circuit below is built using these blocks. Describe its behavior. Also give the circuits common name.


| $X$ | $y$ | Out |  |
| :---: | :---: | :---: | :--- |
| 0 | 0 | $Q_{0}$ |  |
| 1 | 0 | $Q_{0}$ | It's a |
| 0 | 1 | 0 |  |
| 1 | 1 | 1 |  |

## Problem 2 (4 parts, 32 points)

Complete each design below. Be sure to label all signals.
Part A: Complete the following CMOS design. Also Part B: Derive the proper mixed logic expression for the express its behavior.


Out $=$ $A \cdot \bar{B}+C \cdot \bar{D}+\bar{E}$

Out = $\qquad$
Part C: Implement a toggle cell using required latches and basics gates (including XORs). Also complete the behavior table.


| TE | CLR | CLK | Out |
| :---: | :---: | :---: | :---: |
| X | 0 | $\uparrow \downarrow$ | 0 |
| 0 | 1 | $\uparrow \downarrow$ | Q $_{0}$ |
| 1 | 1 | $\uparrow \downarrow$ | $\bar{Q}_{0}$ |


| A | $\mathrm{S}_{1}$ | $\mathrm{~S}_{0}$ | $\mathrm{NS}_{1}$ | $\mathrm{NS}_{0}$ | B |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |

Problem 3 (3 parts, 34 points)
Part A (12 points) Consider a gigabit DRAM chip organized as $\mathbf{6 4}$ million addresses of $\mathbf{1 6}$ bit words. Assume both the DRAM cell and the DRAM chip is square. The column number and offset concatenate to form the memory address. Using the organization approach discussed in class, answer the following questions about the chip. Express all answers in decimal.

| number of columns | $\operatorname{sqrt}\left(2^{30}\right)=2^{15}=32 \mathrm{~K}$ |
| :---: | :---: |
| column decoder required $(n$ to $m)$ | 15 to 32 K |
| type of mux required $(n$ to $m)$ | $32 \mathrm{~K} / 16 \rightarrow 2 \mathrm{~K}$ to 1 |
| number of muxes required | 16 |
| number of address lines in column number | 15 |
| number of address lines in column offset | 11 |
|  |  |

Part B (10 points) Consider a memory system with $\mathbf{5 1 2}$ million addresses of four byte words using DRAM chips organized as $\mathbf{6 4}$ million addresses by 16 bit words

| word address lines for memory system | 29 |
| :---: | :---: |
| chips needed in one bank | 4 bytes $/ 2$ bytes $=2$ chips/bank |
| banks for memory system | $512 M / 64 M=8$ banks $/$ system |
| memory decoder required $(n$ to $m)$ | 3 to 8 |
| DRAM chips required | $2 \times 8=16$ chips/system |

Part C (12 points) For the follow expression, derive a simplified sum of products expression using a Karnaugh Map. Circle and list all prime implicants, indicating which are essential.

$$
\text { Out }=(\bar{A} \cdot B \cdot \bar{D})+(A \cdot C \cdot \bar{D})+(A \cdot B \cdot \bar{C})+(A \cdot C \cdot D)
$$


simplified SOP expression

$A \cdot B+A \cdot C+B \cdot \bar{D}$

Problem 4 (4 parts, 38 points)
Part A (8 points) Convert the following notations:

| binary notation | decimal notation |
| :---: | :---: |
| 10101011.1010 | 171.625 |
| 101001.1110 | 41.875 |
| binary notation | hexadecimal notation |
| 1111000011.1100001111 | $3 C 3 . C 3 C$ |
| 111111.00100011 | 3 F .23 |

Part B (9 points) For the representations below, determine the most positive value and the step size (difference between sequential values). All answers should be expressed in decimal notation. Fractions (e.g., 3/16ths) may be used. Signed representations are two's complement.

| representation | most positive value | step size |
| :---: | :---: | :---: |
| signed integer <br> $(20$ bits $)$. (0 bits) | 512 K | 1 |
| unsigned fixed-point <br> (15 bits) . (5 bits) | 32 K | $1 / 32$ |
| signed fixed-point <br> (10 bits) . (10 bits) | 512 | $1 / 1 \mathrm{~K}$ |

Part C (9 points) A 20 bit floating point representation has a 13 bit mantissa field, a 6 bit exponent field, and one sign bit. Express all answers in decimal.

What is the largest value that can be represented (closest to infinity)?

| $2^{31}=2 B$ |
| :---: |
| $2^{-32}=1 / 4 B$ |
| $\sim 4$ |

Part D (12 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a five bit unsigned fixed-point and five bit two's complement fixed-point representations.


Problem 5 (1 part, 30 points)
Assembly Programming
Part A (30 points) Complete an assembly language routine that computes the average of positives integers in a $\mathbf{2 0 0}$ element array. The array begins at array 5000. Ignore integers in the array that negative (less than zero). Remember that memory is byte addressed and each word in memory is four bytes long (the first word starts at 5000, the second word starts at 5004, etc.) Each time a positive integer is encountered, the number of positive integers (\$5) is incremented. Later $\$ 5$ is used to compute the average. Use the following register assignments: $\$ 1=$ array pointer, $\$ 2=$ end address, $\$ 3=$ current element, $\$ 4=$ current sum, $\$ 5=$ num positive integers, $\$ 6=$ branch predicate. The result (positive integer average) should be stored in $\$ 4$.

| label | instruction | comment |
| :---: | :---: | :---: |
| PosAvg: | addi \$1, \$0, 5000 | \# init array ptr |
|  | addi \$2, \$1, 800 | \# compute end address |
|  | addi \$4, \$0, 0 | \# clear current sum |
|  | addi \$5, \$0, 0 | \# clear number pos ints |
| Loop: | lw \$3, 0 (\$1) | \# load current element |
|  | slt \$6, \$3, \$0 | \# if element < 0 |
|  | bne \$6, \$0, Skip | \# then skip |
|  | add \$4, \$4, \$3 | \# else add to sum |
|  | addi \$5, \$5, 1 | \# increment num pos ints |
| Skip: | addi \$1, \$1, 4 | \# move to next element |
|  | bne \$1, \$2, Loop | \# if not done, loop |
|  | div \$4, \$5 | \# sum / num pos ints |
|  | mflo \$4 | \# move avg to \$4 |
|  | jr \$31 | \# return to caller |

