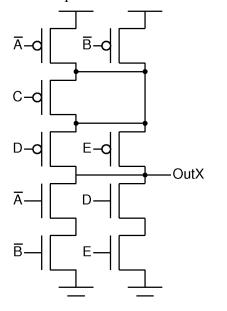
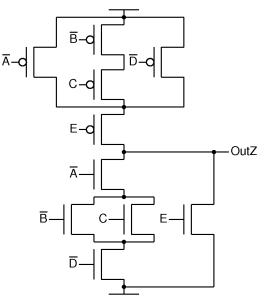
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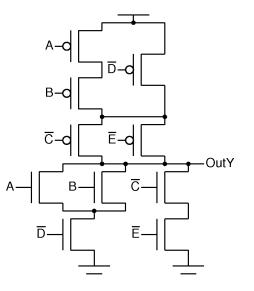
Problem 1 (3 parts, 30 points)

**Incomplete Circuits** 

The three parts below contain (A) a pull up network, (B) a pull down network, and (C) an expression to be implemented. For (A) and (B), complete the missing complementary switching networks so the circuit contains no floats or shorts and write the Boolean expression computed by the completed circuit. For (C), design the entire switching network. Assume the inputs and their complements are available.







OutX =	$(A+B)\cdot(\overline{D}+\overline{E})$
OutY =	$(\overline{A} \cdot \overline{B} + D) \cdot (C + E)$
OutZ =	$(A+B\cdot\overline{C}+D)\cdot\overline{E}$

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Problem 2 (2 parts, 20 points)

Boolean Algebra

Part A (12 points) Transform each of the following Boolean expressions to a equivalent form where they contain only AND operations. Do not implement.

$$OUT_{X} = \overline{\overline{A} \cdot B} + C \cdot \overline{D} \qquad \qquad \overline{\overline{A} \cdot B} \cdot \overline{C \cdot \overline{D}}$$

$$OUT_{Y} = \overline{\overline{A} \cdot \overline{B} + \overline{C} \cdot \overline{D} + \overline{E}} \qquad \qquad \overline{\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E}}$$

Part B (8 points) Derive the canonical product of sums (using maxterms) expression using the behavior expressed in the truth table.

В	С	F <sub>(A,B,C)</sub>
0	0	0
0	0	1
1	0	0
1	0	1
0	1	0
0	1	0
1	1	1
1	1	1
	0 0 1 1 0 0	0 0   0 0   1 0   1 0   0 1   0 1   1 1

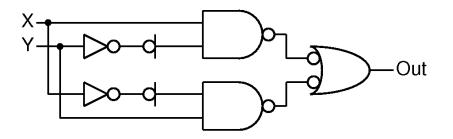
 $\operatorname{POS}_{(\text{maxterms})} = (A + B + C) \cdot (A + \overline{B} + C) \cdot (A + B + \overline{C}) \cdot (\overline{A} + B + \overline{C})$ 

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## Problem 3 (2 parts, 26 points)

Mixed Logic Design

Part A (10 points) Implement a two-input odd parity gate (XOR) using basic gates and inverters to minimize implementation cost. Use proper mixed logic notation. Assume only true inputs (X and Y) are available. Tally the implementation transistors. Hint:  $Out = X \cdot \overline{Y} + \overline{X} \cdot Y$ 



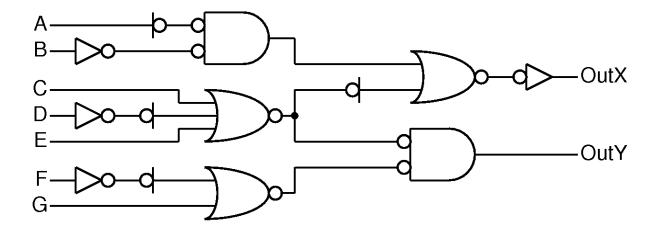
```
# transistors =
```

# transistors =

3 x 4 + 2 x 2 = 12 + 4 = 16

Part B (16 points) Implement the follow expression using basic gates and inverters to minimize implementation cost. Use proper mixed logic notation. Assume only true inputs are available. *Do not modify the expressions being implemented*. Show the implementation cost (in transistors).

$$OUT_{X} = \overline{A} \cdot B + (\overline{C} + \overline{D} + \overline{E})$$
$$OUT_{Y} = (C + \overline{D} + \overline{E}) \cdot (\overline{F} + \overline{G})$$

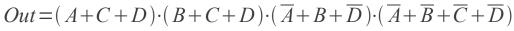


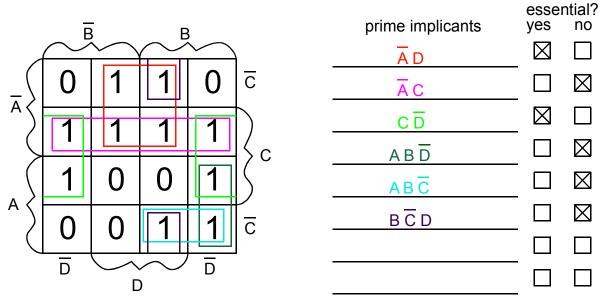
 $1 \times 6 + 4 \times 4 + 4 \times 2 = 6 + 16 + 8 = 30$ 

Problem 4 (2 parts, 24 points)

Karnaugh Maps

Part A (12 points) For the follow expression, derive a simplified *sum of products* expression using a Karnaugh Map. Circle and list *all* prime implicants, indicating which are essential.





simplified SOP expression

A 1	D+C			$\mathbf{\mathbf{n}}$
$\Delta \cdot I$	) + (	$\cdot $	$\Delta \cdot \mathbf{R}$	
				$\mathbf{U}$

Part B (12 points) For the behavior in the map below, derive a simplified *product of sums* expression. Circle and list all prime implicants, indicating which are essential.

1					1 ,	·	prime implicants	esse yes ⊠	ntial? no
1					Ì		A + B		
_ \	0	0	1	X <sub>0</sub>	<u></u>		C + D	$\square$	
Ā	<b>X</b> 0	$\mathbf{\cap}$	1	1	$\square$				
(				-	ζc				
	1	1	1	1	$\left  \right\rangle$				
A		1	4	V	-				
(	0		l	Λ <sub>0</sub>					
	D		$\sim$	D					
simpli	fied POS	S expres	ssion _			( <b>A</b> -	$+B)\cdot(C+D)$		