Instructions: This is a closed book, closed note exam. Calculators are not permitted. If you have a question, raise your hand and I will come to you. Please work the exam in pencil and do not separate the pages of the exam. For maximum credit, show your work.
Good Luck!

Your Name (please print) $\qquad$


Problem 1 (3 parts, 24 points)
Part A ( 6 points) Define a 1 to 2 decoder by completing the behavior table.

| IN | EN | O 0 | O 1 |
| :---: | :---: | :---: | :---: |
| X | 0 |  | IN O0 <br> 1 to 2 <br> decoder <br> EN <br> 0 |
| 1 | 1 |  |  |

Part B (8 points) Implement a 1 to 2 decoder using basic gates. Assume only true (noncomplemented) inputs are available. Label all inputs and outputs.

Part C (10 points) Using only the three 1 to 2 decoders shown below, implement a 2 to 4 decoder with an enable. Label the decoder inputs $\left(\mathrm{IN}_{1}, \mathrm{IN}_{0}, \mathrm{EN}\right)$ and outputs (O0, O1, O2, O3).


Problem 2 (2 parts, 18 points)
"Get your priorities right!"
Consider a priority encoder with the following behavior:

| $\mathrm{In}_{3}$ | $\mathrm{In}_{2}$ | $\mathrm{In}_{1}$ | $\mathrm{In}_{0}$ | Valid | $\mathrm{O}_{1}$ | $\mathrm{O}_{0}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | X | X |
| X | X | X | 1 | 1 | 0 | 0 |
| X | X | 1 | 0 | 1 | 0 | 1 |
| X | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 |

Part A (8 points) List the inputs $\left(\operatorname{In}_{0}, \operatorname{In}_{1}, \mathrm{In}_{2}\right.$, and $\left.\mathrm{In}_{3}\right)$ in increasing priority.


Part B ( 10 points) Express the behavior of $\mathrm{O}_{0}$ in the map below. Derive a simplified sum of products expression using a Karnaugh Map. Circle and list the prime implicants, indicating which are essential. Then write the simplified SOP expression.


Problem 3 (4 parts, 40 points)
Number Systems \& Arithmetic
Part A (10 points) Convert the following notations:

| binary notation | decimal notation |
| :---: | :---: |
| 11011011. |  |
| 1011100.1101 | 27.625 |
|  | hexadecimal notation |
| binary notation |  |
| 100100101.110111 | CB4.2B1 |

Part B (12 points) For the 22 bit representations below, determine the most positive value and the step size (difference between sequential values). All answers should be expressed in decimal notation. Fractions (e.g., 3/16ths) may be used. Signed representations are two's complement.

| representation | most positive value | step size |
| :---: | :--- | :--- |
| unsigned integer |  |  |
| (22 bits) . ( 0 bits) |  |  |
| signed fixed-point |  |  |
| (18 bits) . (4 bits) |  |  |
| signed fixed-point |  |  |
| (14 bits) . 8 bits) |  |  |
| signed fixed-point |  |  |
| $(11$ bits) . (11 bits) |  |  |

Part C (6 points) A 16 bit floating point representation has a 10 bit mantissa field, a 5 bit exponent field, and one sign bit.

What is the largest value that can be represented (closest to infinity)?
What is the smallest value that can be represented (closest to zero)?
2
2
How many decimal significant figures are supported?
Part D (12 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a five bit unsigned fixed-point and five bit two's complement fixed-point representations.


Problem 4 (3 parts, 18 points)
"Does this register?"
Part A (6 points) Express the behavior of the circuit below. Use standard symbols ( $0,1, \mathrm{X}, \mathrm{Z}_{0}$, $\mathrm{Q}_{0}$, etc.). Then name the circuit.


| A | B | $X$ | $Y$ |
| :---: | :---: | :---: | :---: |
| 0 | 0 |  |  |
| 1 | 0 |  |  |
| 0 | 1 |  |  |
| 1 | 1 |  |  |

This circuit is a $\qquad$
Part B (6 points) Implement a register below using only latches, pass gates, and inverters (all in icon form). Complete the behavior table at right. Recall that the CLK signal indicates a full $\Phi_{1} \Phi_{2}$ cycle; so the output should be the value at the end of a cycle (for the given inputs).

| In | WE | Clk | Out | $\overline{\text { Out }}$ |
| :---: | :---: | :---: | :---: | :---: |
| $A$ | 0 | $\uparrow \downarrow$ |  |  |
| $A$ | 1 | $\uparrow \downarrow$ |  |  |

In


Part C (6 points) Assume the following signals are applied to your register. Draw the output signal Out. Draw a vertical line where In is sampled. Draw crosshatch where Out is unknown.


