Problem 1 (4 parts, 32 points)
Implementation Bonanza
For each part implement the specified device. Label all inputs and outputs.

Part A (8 points) Implement the expression below using N and P type switches.

$$
O U T_{X}=A \cdot \bar{B} \cdot C+\bar{D}+E
$$



Part C (8 points) Implement a 2 to 4 decoder with enable using basic gates.





Part B (8 points) Implement the expression in mixed logic notation using NAND gates.

$$
O U T_{Y}=\bar{A} \cdot B+(\overline{C+\bar{D}})
$$



Part D (8 points) Write a POS expression for a two-input XOR (odd parity) using maxterms.

| A | B | A XOR B |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

$$
\text { Out }=(A+B) \cdot(\bar{A}+\bar{B})
$$

Problem 2 ( 6 parts, 32 points)
Alien Software
SETI has just received an interesting message from deep space. While the comments are written in an alien tongue, they appear to write programs in MIPS assembly. Intergalactic scientists have only been able to decode the register assignments. Computer engineers must take it from there.

```
# INPUTS: $1= num elements, $2= array A pointer, $3= array B pointer,
# OUTPUT: $6=result, WORKING: $4= InA/diff, $5= InB/pred,
```

| $\#$ | label | instruction | comment |
| :---: | :--- | :--- | :--- | :--- |
| L1 | Whats It: | sub $\$ 6, \$ 6, \$ 6$ | $\#$ clear max difference |
| L2 | Loop: | lw $\$ 4, \quad(\$ 2)$ | $\#$ load A element |
| L3 |  | lw $\$ 5,(\$ 3)$ | $\#$ load B element |
| L4 |  | sub $\$ 4, \$ 4, \$ 5$ | $\#$ compute difference |
| L5 |  | slt $\$ 5, \$ 4, \$ 0$ | $\#$ if difference >= 0 |
| L6 |  | beq $\$ 5, \$ 0$, Skip1 | $\#$ then skip |
| L7 |  | sub $\$ 4, \$ 0, \$ 4$ | $\#$ otherwise negate |
| L8 | Skip1: | slt $\$ 5, \$ 6, \$ 4$ | $\#$ if MaxDif >= difference |
| L9 |  | beq $\$ 5, \$ 0$, Skip2 | $\#$ then skip |
| L10 |  | add $\$ 6, \$ 4, \$ 0$ | $\#$ otherwise update MaxDif |
| L11 | Skip2: | addi $\$ 2, \$ 2,4$ | $\#$ increment A ptr |
| L12 |  | addi $\$ 3, \$ 3,4$ | $\#$ increment B ptr |
| L13 |  | addi $\$ 1, \$ 1,-1$ | $\#$ decrement element count |
| L14 |  | bne $\$ 1, \$ 0$, Loop | $\#$ loop if not done |
| L15 |  | jr $\$ 31$ | $\#$ return to caller |

Part A - E (26 points) Decode the abstract purpose of code in terms of the defined variable names. Don't transliterate instructions to words.

| A: What does L1 accomplish? | B: What math function do L5-L7 implement? |
| :--- | :---: |
| It initializes Result to 0 | absolute value |
| C: Why is Result updated (in terms of InA, InB)? | D: What is the branch offset in L14 (in bytes)? |
| InA - InB $\mid$ is greater than the current <br> maximum difference. | -52 bytes ( -13 instructions) |
| E: What does the overall function compute? |  |
| This function finds the largest difference in corresponding value in two equal sized <br> arrays. |  |

Part F (6 points) Another routine calls WhatsIt below. Add missing instructions to preserve and restore its return address on the stack. Recall that $\$ 29$ is the stack pointer.

| label | instruction | comment |
| :--- | :--- | :--- |
|  | addi \$29, \$29, -4 | \# push return address ... |
|  | sw \$31, (\$29) | \# ... on stack |
|  | jal WhatsIt | \# call WhatsIt |
|  | lw \$31, (\$29) | \# pop return address ... |
|  | addi \$29, \$29, 4 | \# ... off stack |

Problem 3 (3 parts, 24 points)
Agents changed the matrix
Part A (8 points) Consider the circuit below. Complete the truth table. Then state what logical function this circuit implements.


This wacky circuit is a $\qquad$
XNOR (even parity)
Part B (8 points) Consider four different function definitions below. The symbolic value $A$ is presented at its input. The control input and resulting out are shown in the truth table. Name the gate, building block, or storage device that implements each definition.


| In | $C$ | (2) | $(3)$ | $(4)$ | $(5)$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $A$ | 0 | $Q_{0}$ | 1 | 0 | $A$ |
| $A$ | 1 | $A$ |  | $A$ |  |

(2)
transparent latch
(3) NAND
(4) AND
(5) $X O R$

Part C (8 points) Blocks from part B are used to create a new module below. The symbolic values $X$ and $Y$ are presented at its inputs along with a two-phase clock. Complete the truth table and give its functional name.


Problem 4 (2 parts, 28 points)
Microcode
Using the supplied datapath, write microcode fragments to accomplish the following procedures. Express all values in hexadecimal notation. Use ' X ' when a value is don't cared. For maximum credit, complete the description field.
Part A (14 points) $\quad R_{7}=\frac{3 \times R_{5}}{16}-256 \times R_{6} \quad$ Modify only $\mathbf{R}_{5}, \mathbf{R}_{6}$ and $\mathbf{R}_{7}$.

| \# | X | $Y$ | $z$ | rwe | ${ }_{\text {im }}^{\text {en }}$ | im va | $\begin{aligned} & a u \\ & e n \end{aligned}$ | $\bar{a}$ | $\begin{aligned} & l u \\ & e n \\ & e \end{aligned}$ | If | su <br> $e n$ | st | $\begin{gathered} l d \\ e n \end{gathered}$ | $\begin{aligned} & s t \\ & e n \\ & e n \end{aligned}$ | $r$ $-w$ | msel | description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 5 | 5 | 7 | 1 | 0 | X | 1 | 0 | 0 | X | 0 | X | 0 | 0 | X | 0 | R7 - R5 + R5 |
| 2 | 7 | 7 | 5 | 1 | 0 | X | 1 | 0 | 0 | X | 0 | X | 0 | 0 | X | 0 | R7 $\square$ R7 + R5 |
| 3 | 7 | x | 7 | 1 | 1 | 4 | 0 | X | 0 | X | 1 | 1 | 0 | 0 | X | 0 | R7 $\mathrm{R}^{\text {R }}$ >> 4 |
| 4 | 6 | X | 6 | 1 | 1 | FFF8 | 0 | X | 0 | X | 1 | 1 | 0 | 0 | X | 0 | R6 - R6 << 8 |
| 5 | 7 | 6 | 7 | 1 | 0 | X | 1 | 1 | 0 | X | 0 | X | 0 | 0 | X | 0 | R7 - R7-R6 |
| 6 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 7 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Part B (14 points) Write a microcode sequence that loads a 32 bit word from memory location $0 \times 4000$, unpacks and averages two 15 bit unsigned values ( $A$ and $B$ ), and then stores the result back to memory location $0 \times 4000$. Assume the most significant two bits of the register are zero.
Modify only $\mathbf{R}_{1}, \mathbf{R}_{\mathbf{2}}$, and $\mathbf{R}_{\mathbf{3}}$.


| \# | $X$ | $Y$ | Z | rwe | ${ }_{\text {i }}^{\text {im }}$ | im va | $a u$ $e n$ en | $\stackrel{\square}{a}$ | lu <br> $e n$ | If | su $e n$ | st | $l d$ $e n$ | $s t$ $e n$ | $r$ $-w$ | msel | description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | X | X | 1 | 1 | 1 | 4000 | 0 | X | 1 | c | 0 | X | 0 | 0 | x | 0 | R1 $\square 0 \times 4000$ |
| 2 | 1 | X | 2 | 1 | 0 | x | 0 | x | 0 | x | 0 | X | 1 | 0 | 1 | 1 | R2 $\square$ mem[R1] |
| 3 | 2 | X | 3 | 1 | 1 | 7FFF | 0 | x | 1 | 8 | 0 | x | 0 | 0 | x | 0 | R3 $\square$ R2 \& 0x7FFF |
| 4 | 2 | x | 2 | 1 | 1 | F | 0 | $x$ | 0 | x | 1 | 0 | 0 | 0 | x | 0 | R2 $\quad$ R2 >> 15 |
| 5 | 2 | 3 | 2 | 1 | 0 | X | 1 | 0 | 0 | $x$ | 0 | x | 0 | 0 | x | 0 | R2 $\square$ R2 + R3 |
| 6 | 2 | X | 2 | 1 | 1 | 1 | 0 | X | 0 | X | 1 | 1 | 0 | 0 | X | 0 | R2 $\quad$ R2 >> 1 |
| 7 | 1 | 2 | $x$ | 0 | 0 | X | 0 | x | 0 | x | 0 | x | 0 | 1 | 0 | 1 | $\operatorname{mem}[R 1] \square R 2$ |
| 8 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Problem 5 (4 parts, 40 points)
This and That
Part A (9 points) Consider the instruction set architecture below with fields containing zeros.

| 00000 | 0000000 | 0000000 | 000000000000000 |
| :---: | :---: | :---: | :---: |
| opcode | dest. reg. | source 1 reg. | immediate value |

What is the maximum number of opcodes?

$$
2^{5}=32
$$

What is the number of registers?
$2^{7}=128$
What is the range of the signed immediate value?

$$
2^{15}= \pm 16 K
$$

Part B (9 points) List three differences between a branch and a jump in the MIPS ISA.
1: Branches are conditional; jumps are unconditional.
2: Branch offsets are relative, jump targets are absolute.
3: Branch range $\pm 32 \mathrm{~K} \mathrm{I}_{1} \pm 128 \mathrm{Kbytes} ;$ jump range 0-64M I, 0-256Mbytes
Part C (12 points) For 32 bit representations below, determine the most positive value and the step size (difference between sequential values). All answers should be expressed in decimal notation. Fractions (e.g., 3/16ths) may be used. Signed representations are two's complement.

| representation | most positive value | step size |
| :---: | :---: | :---: |
| unsigned integer <br> $(32$ bits $)$. 0 bits $)$ | 4 billion | 1 |
| signed fixed-point <br> $(28$ bits) . (4 bits) | 128 million | $1 / 16$ |
| signed fixed-point <br> $(25$ bits $) .(7$ bits) | 16 million | $1 / 128$ |
| signed fixed-point <br> $(21$ bits) . (11 bits) | 1 million | $1 / 2 \mathrm{~K}$ |

Part D (10 points) Consider a memory system with $\mathbf{2 5 6}$ million addresses of $\mathbf{8}$ byte words using DRAM chips organized as $\mathbf{1 6}$ million addresses by $\mathbf{3 2}$ bit words.

| word address lines for memory system | $\log _{2}(256 \mathrm{M})=28$ |
| :---: | :---: |
| chips needed in one bank | 8 bytes $/ 4$ bytes $(32$ bits $)=2$ chips |
| banks for memory system | $256 \mathrm{M} / 16 \mathrm{M}=2^{8} / 2^{4}=2^{4}=16$ banks |
| memory decoder required ( $n$ to $m$ ) | 4 to 16 |
| total memory system size (in bytes) | $256 \mathrm{M} \times 8=2^{28} \times 2^{3}=2^{31}=2$ GBytes |

